REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
02/08/2011	Annual	07/15/2007 - 07/14/2009

4. TITLE AND SUBTITLE

High Performance Crystalline Organic Transistors and Circuit

5a. CONTRACT NUMBER
N/A

5b. GRANT NUMBER
FA9550-07-1-0553, P00001

5c. PROGRAM ELEMENT NUMBER
N/A

6. AUTHOR(S)

Ananth Dodabalapur

5d. PROJECT NUMBER
FA9550-07-1-0553

5e. TASK NUMBER
N/A

5f. WORK UNIT NUMBER
N/A

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

The University of Texas at
Austin, 10100 Burnet Road,
Bldg. 160, Austin, TX 78758

8. PERFORMING ORGANIZATION REPORT NUMBER

E

UT OSP # 200701278

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Dr. Charles Lee, AFOSR
875 N. Randolph St., Rm 3112
Arlington, VA
Charles.lee@afosr.af.mil

10. SPONSOR/MONITOR'S ACRONYM(S)
DOD-Air Force

11. SPONSOR/MONITOR'S REPORT NUMBER(S)
AFRL-OSR-VA-TR-2011-0012

12. DISTRIBUTION / AVAILABILITY STATEMENT

Distribution A: Approved for Public Release

13. SUPPLEMENTARY NOTES

14. ABSTRACT

We have examined the best available small molecule crystalline organic semiconductors as active layers in thin-film transistors. We have optimized the field-induced conductance, a figure of merit that will relate directly to circuit speeds. A simple figure of merit – the product of the field-effect mobility and effective relative dielectric constant of the gate insulator (or mobility times the product of capacitance per unit area and total insulator thickness for bilayers)has been used to compare our devices with all the published work in the literature up until the project ending. The best semiconductor-insulator combination was found to a porphryn semiconductor in conjunction with a bilayer gate insulator consisting of ~ 100 nm Ta_2O_3 and 2.3 nm SiO_2. We also discuss the physics of charge trapping at various semiconductor-dielectric interfaces.

15. SUBJECT TERMS
Organic transistor, high-k dielectric, bilayer dielectric, flexible electronics, field-effect transistor

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE		22	Ananth Dodabalapur
					19b. TELEPHONE NUMBER *(include area code)* 512-232-1890

INTRODUCTION

The majority of reported organic transistors employ a relatively thick gate dielectric layer, on the order of 100 nm or greater. The traditional choice of insulator for use in material development and basic experiments is thermally grown silicon dioxide (SiO2), due to the excellent quality of the film. Unfortunately, the relatively low dielectric constant of SiO2 leads to small capacitances for these thick films. This results in large voltages being necessary for adequate device operation. The effect is further exacerbated by the carrier concentration dependent mobility exhibited by most organic semiconductors.

Devices with high operating voltages, often in excess of 30 volts, work perfectly fine for most theoretical studies and experiments. Problems arise, however, when integrating these devices into circuits and other applications. In order to reduce these operating voltages to more manageable levels, the capacitance of the dielectric layer must be increased. There are two methods to increase this capacitance. Either the thickness of the dielectric layer can be decreased, or a material with a higher dielectric constant can be employed.

Decreasing the thickness of the dielectric layer is a common approach. This can increase the effect of defects such as pinholes in the insulator. While this poses difficulty in the manufacturing process, these problems can be overcome. Of greater difficulty is electrical breakdown within the insulator. This will limit the voltage that may be applied.

Increasing the dielectric constant of the insulator poses unique challenges as well. Many materials with a high dielectric constant exist that are suited to thin film deposition. Such materials increase the capacitance of the insulating layer while maintaining a large breakdown voltage. They often consist of a highly polar metal oxide. Aluminum oxide (Al_2O_3), tantalum oxide (Ta_2O_5), and hafnium oxide (HfO_2) all may present dielectric constants greater than 10. These materials are traditionally deposited through chemical vapor deposition methods (CVD), electron-beam evaporation, sputtering, or atomic layer deposition (ALD). These processes are expensive and typically incompatible with roll to roll processing techniques.

2 ZIRCONIUM OXIDE GATE DIELECTRIC

2.1 Device fabrication

One particular choice of high-k dielectric is zirconium oxide (ZrO_2). Typically sputtered, recent work has developed a sol-gel deposition method that allows this material to be deposited from solution[1]. This allows the material to be printed or otherwise incorporated into typical organic electronic fabrication processes. Though originally intended for use with inorganic metal-oxide semiconductor based thin film transistors, a process to spin-coat thin ZrO2 layers has been optimized within our research group[2]. By incorporating this material into pentacene-based OFETs, low voltage operation is possible.

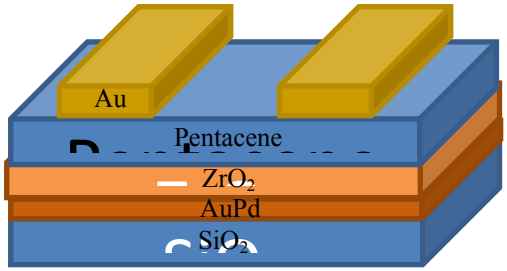

Figure 1: Device structure for a low voltage pentacene OFET using a ZrO_2 gate dielectric.

For a substrate, a silicon (Si) wafer was used. This provided a stable, extremely flat surface. A metal gate was employed rather than simply use a heavily doped Si wafer as both substrate and gate, as seen in Chapter 2. This provides a reflective layer beneath the device, removing effects caused by light absorption in the underlying Si layer. These effects can alter the device characteristics, particularly the threshold voltage. A SiO_2 layer was grown on top of the wafer, providing an insulating buffer layer. A thin titanium (Ti) adhesion layer and a gold-palladium ($Au_{0.6}Pd_{0.4}$) gate layer were deposited by electron beam evaporation on top of the buffer layer.

A 16% molecular weight solution of zirconium chloride ($ZrCl_4$) and $Zr(OCH(CH_3)_2)_4 \cdot (CH_3)_2CHOH$ in 2-methoxyethanol at a 1:1 molar ratio was then spun at a speed of 4000 rpm for 60 seconds under a nitrogen (N_2) atmosphere. This film was left for one hour in N_2 to evaporate any remaining solvent then annealed at 350 degrees Celsius for one hour in ambient air. A second layer of ZrO_2, deposited under identical conditions, was then added. This second layer addressed uniformity issues with the first

film. Bilayer dielectrics exhibit lower defect-related leakage effects, as pinholes or other defects in one layer may be isolated by the other layer.

350 Å of pentacene was thermally evaporated on the ZrO_2 dielectric at a rate of 0.1 Å/s under a pressure $<5x10^{-7}$ torr and a substrate temperature of 70 degrees Celsius. Gold source and drain electrodes were then thermally evaporated on top of the pentacene layer using a shadow mask as a pattern. The gold was deposited at a rate of 0.1 Å/s for the first 50 Å, then at a rate of 1.0 Å/s for the remaining 950 Å, for a total thickness of 1000 Å.

2.2 Device Characteristics

These devices were tested under vacuum, at a pressure of $<1x10^{-3}$ torr, using an Agilent 4155C parameter analyzer and an HP 4284a LCR meter. Figures 3.3 and 3.4 display the output and transfer characteristics for a 50um channel length device, respectively. With turn on voltages of less than -1V, these devices operated quite effectively in the 0 to -5V range. Leakage currents through the gate dielectric were minimal, averaging less than 1 nA when 5 V was applied voltage across the insulator.

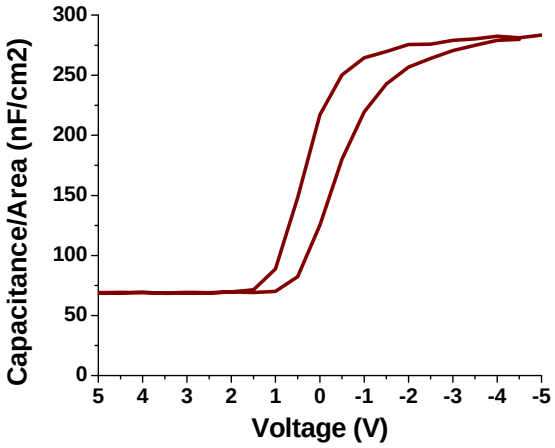

Figure 2: Capacitance plotted against applied voltage for a metal-insulator-semiconductor structure at low frequencies (100 Hz). Under accumulation, the capacitance increases to 280 nF/cm^2, corresponding to the capcitance of the ZrO_2 dielectric. Significant hysteresis is shown.

Figure 2 shows a plot of capacitance against applied DC voltage for a metal-insulator-semiconductor structure. Because pentacene operates through majority carrier accumulation, when a positive bias is applied to the gate electrode, there are no mobile carriers present in the pentacene layer. This means that the capacitance seen corresponds to the capacitance of the pentacene-ZrO_2 stack. When a negative gate voltage is applied, holes begin to accumulate at the interface, and the measured capacitance begins to correspond to the ZrO_2. From this plot, we can calculate the capacitance per unit area of our ZrO2 dielectric layer to be 280 nF/cm^2.

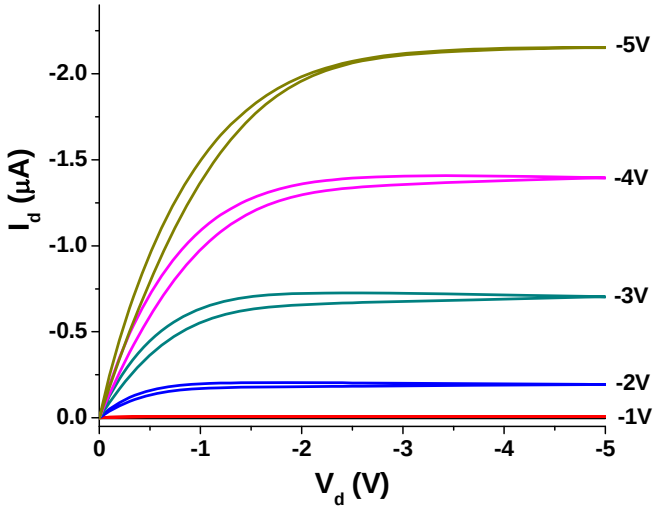

Figure 3: Output characteristics for a 50um channel length pentacene transistor on ZrO2.

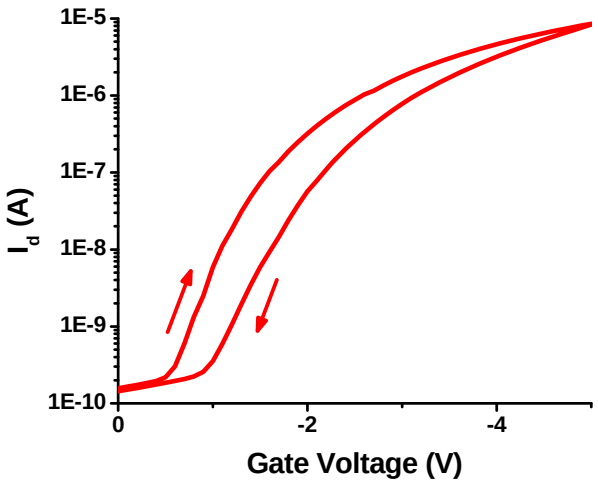

Figure 4: Transfer characteristics of a 50um pentacene on ZrO2 transistor. A large hysteresis can be seen between forward and reverse sweeps.

The large hysteresis seen in these graphs is due to a phenomenon known as the bias stress effect. This effect is characterized by a shift in threshold voltage with time under an applied gate voltage. Therefore the hysteresis seen in these curves is not truly hysteresis due solely to the direction of the voltage sweep, but is rather a function of the time taken to sweep these voltages.

An effective field effect mobility can be extracted from this transfer curve. In the saturation regime, the carrier mobility can be related to the differential current caused by a change in gate voltage as:

$$\mu_{FET} = \frac{2L}{WC_i}\left[\frac{\partial\sqrt{I_d}}{\partial V_g}\right]^2$$

By calculating this value at each point along the transfer curve, a plot of field effect mobility versus applied gate voltage can be extracted. Figure 3.4 shows a plot of mobility obtained from a transfer curve obtained with a stepped gate voltage. The extracted mobility varies greatly between forward and backward sweeps towards the higher voltages, with a drastic singularity present at V_g=-5V. This difference is an artifact introduced by the bias stress effect, where on the forward sweep the differential current appears lower than it should, and the backwards sweep appears larger.

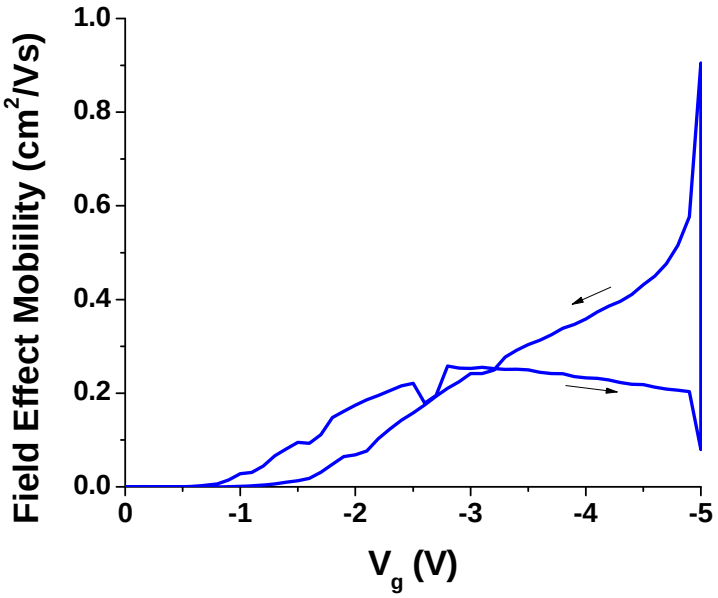

Figure 5: Mobility calculated from the saturation FET equations plotted against applied gate voltage from transfer curves obtained through application of a stepped gate voltage. Bias stress effects distort the results.

In order to reduce these effects when testing the device, a series of transfer curves were extracted using the 4155C to apply voltage pulses to the gate instead of applying a constant voltage. One such curve can be seen in Figure 6. In this mode, the noise floor of the 4155C rises significantly, making accurate determination of the turn-on voltage and sub-threshold swing impossible. It does, however, allow points obtained at higher voltages to be extracted with minimal effect from bias stress.

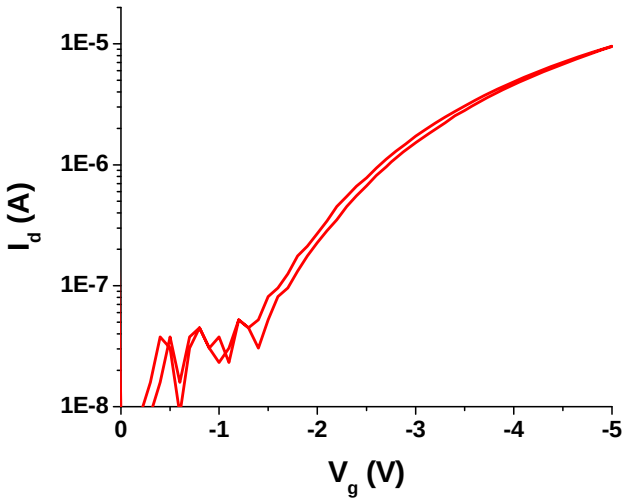

Figure 6: Transfer curve for a 50um pentacene on ZrO_2 device measured using a pulsed gate voltage.

Figure 7 displays field effect mobility values calculated from the transfer curves shown in Figure 6. There is a significant amount of noise in the results, but the greatly reduced hysteresis allows it to become evident that the field effect mobility increases to a value of roughly 0.3 cm^2/Vs at higher carrier concentrations. The extraction of an accurate mobility value from this device allows us to compare the quality of the pentacene layer with the semiconductor in devices with different structures.

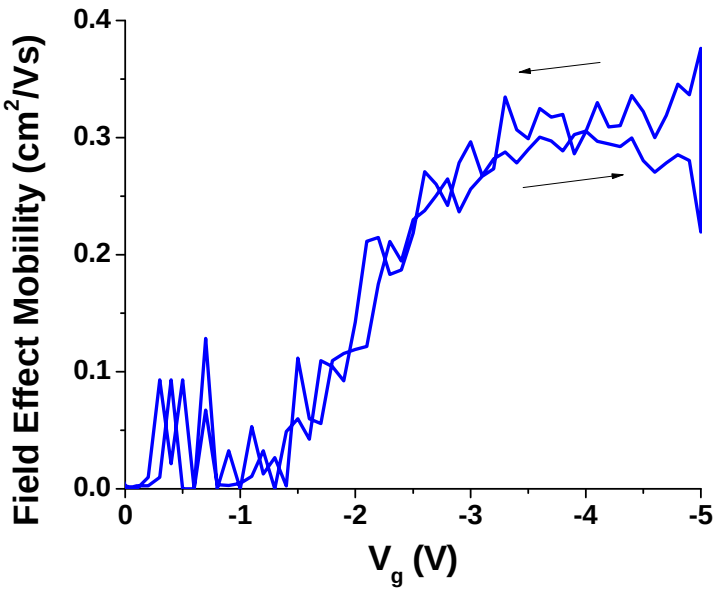

Figure 7: Field effect mobility for the saturation regime plotted against applied gate voltage, calculated from transfer curves obtained with a pulsed gate voltage.

3 Reducing the Bias Stress Effect

3.1 Bias Stress

This reduction in drain current under prolonged gate bias is seen across virtually all organic transistors. It causes problems, however, when attempting to fashion useful circuits, sensors, or other useful devices. This effect does not appreciably change the mobility of carriers within the channel. Rather, it reduces the current by increasing the turn-on voltage. The increase in turn-on voltage is due to charge carriers becoming trapped within the channel, effectively screening a portion of the gate voltage.

A variety of mechanisms have been proposed to explain the origin of these traps, including bipolaron formation, moisture incorporation, oxygen degradation, and other effects. The Phillips Corporation and others have theorized that these trapped charges may lie not within the semiconductor, but within the dielectric itself. The model used by Phillips accurately predicts a bias stress effect caused by moisture in bottom gate devices fabricated using a silicon dioxide gate dielectric[3]. In this model, electrolysis of even a very slight amount of water releases protons that may diffuse into the first 10 to 20 nm of the SiO_2.

Experiments on single crystal organic FETs insulated from the surrounding atmosphere have also displayed a significant bias stress effect. This has been attributed to an overlap in energy between the mobile band tail states in the semiconductor and trap states in the insulator caused by disorder. Charges in the semiconductor are able to transfer into the available states within the insulator, albeit at a very slow rate governed by the hopping mobility of carriers within the insulator, often of the order of 10^{-10} cm^2/Vs or lower[4].

3.2 Device Structure

Regardless of the source, these deep trap states have a large effect on the response of a device. In order to achieve a stable device response, this issue must be dealt with. The most promising methods involve either encapsulation of the active material in order to reduce environmental effects[5] or choosing a gate insulator that exhibits better bias

stress characteristics[6]. Hydrophobic gate insulators reduce the effect of moisture by repelling water molecules from the surface[3].

As seen in Figure 8, the bias stress effects within the aforementioned devices display a large environmental dependence. The bias stress effect was first measured under vacuum after one hour. After one minute of applied gate bias, the current fell to roughly 20% of its starting value. After four hours in vacuum, the bias stress effect only reduced the current to 60% of its initial value after one minute of applied bias. One possible cause is the removal of moisture over time.

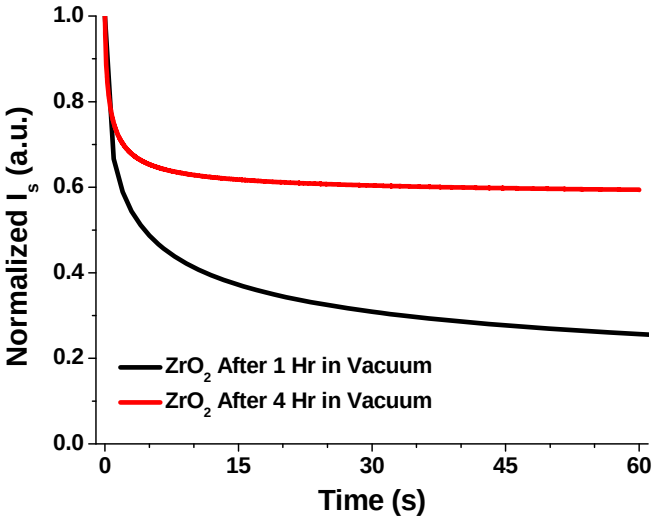

Figure 8: Bias stress effect in Pentacene transistor with ZrO_2 dielectric. Prolonged exposure to vacuum reduces the magnitude of the bias stress effect.

In order to reduce this effect, it would be beneficial to choose a different gate insulator. Poly(vinyl cinnamate) (PVCn) is a hydrophobic insulating material that is

easily processed from solution. When cross-linked, PVCn becomes insoluble in a variety of solvents. This allows the use of photolithography to define patterns on the surface. This cross-linking process also drastically increases the field at which the material enters breakdown [PVCn transistors]. Devices fabricated using PVCn as gate insulators demonstrate a dramatically reduced bias stress effect. However, the use of this structure can introduce significant issues.

The most important issue presented by the use of a PVCn gate dielectric is the relatively low-k nature of the material. The relative dielectric constant of the material is similar to SiO_2, increasing the voltages required to operate the device. The material is also very soft, making the film less robust and more susceptible to defects such as pinhole effects and particle contamination that can often bridge the entire film, resulting in significantly increased leakage currents and lowering the breakdown voltage. In order to combat these effects, a thinner layer must be deposited, increasing the operating voltage further.

The solution explored here incorporates the best features of both PVCn and ZRO_2 to create a stable bilayer insulating film. Figure 3.9 shows the device structure, where an extremely thin layer of PVCn (5 to 10 nm) is deposited on top of a single ZRO_2 layer. The PVCn layer is deposited by spin-casting a solution of 0.5% by weight PVCn in a solvent of cyclopentanone at 4,000 rpm for 60 seconds. This film is then annealed at 100 degrees Celsius for one hour in order to fully remove all of the solvent. A brief UV exposure to a 245nm source served to fully crosslink the film. The rest of the device structure and processing is identical to the previously mentioned pentacene devices

employing purely ZRO_2 gate dielectrics. Capacitance vs. voltage curves of this MIS structure show that this bilayer dielectric has a capacitance per unit area of 230 nF/cm^2. This is only slightly lower than the 275 nF/cm^2 obtained in the purely ZrO2 dielectric.

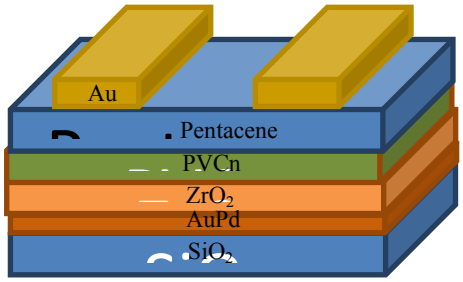

Figure 9: Pentacene device structure using a bilayer of ZrO_2 and PVCn as the gate insulator.

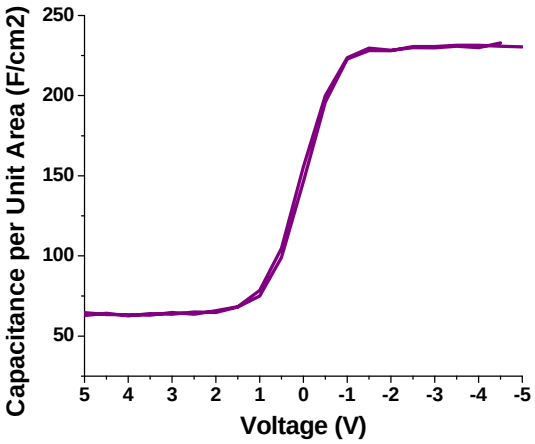

Figure 10: Capacitance-Voltage curve for a MIS structure with a pentacene active layer and a ZrO_2/PVCn bilayer dielectric. Dielectric capacitance of 230 nF/cm^2 is obtained.

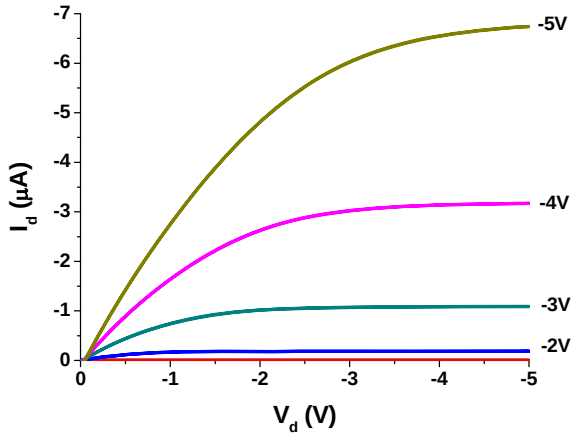

Figure 11: Output curves for a pentacene transistor with a ZrO_2/PVCn bilayer dielectric displaying operation below -5V.

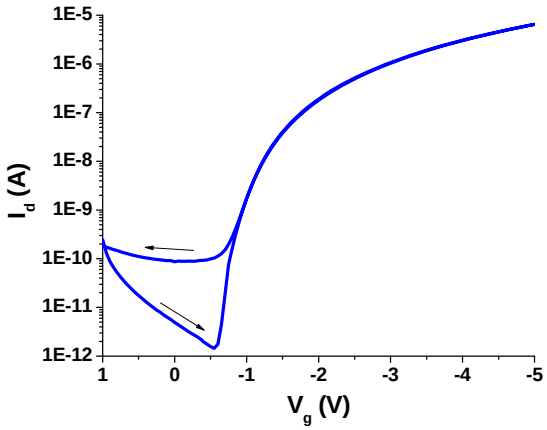

Figure 12: Transfer curve for a pentacene transistor with a ZrO_2/PVCn bilayer dielectric showing minimal hysteresis in the operation above threshold. V_d was kept at -5V.

Output and transfer curves are displayed for this device structure in Figures 11 and 12, respectively. The transfer curves display only an extremely slight hysteresis. Figure 13 displays the field effect mobility of carriers within the device. Due to the extremely low hysteresis, the pulsed gate technique was not necessary in order to calculate the carrier mobility. Hole mobilities approaching 0.3 cm^2/Vs are seen at gate voltages of -5V.

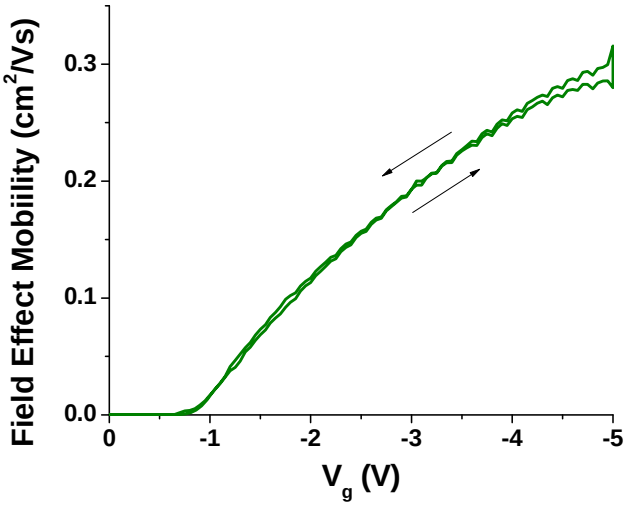

Figure 13: Field effect mobility for a pentacene device with a ZrO_2/PVCn bilayer dielectric. Saturation mobilities up to 0.28 cm^2/Vs are obtained.

Figure 14 compares the change in drain current over time due to the bias stress effect in devices both with and without the PVCn bilayer. The drain current actually increases with time in the device with the PVCn bilayer, reflecting a threshold shift in the opposite direction of the applied gate voltage. This shift, however, accounted for a

change in drain current of only about 5% over a 5 minute period. This is significantly less than the 80% drop seen using a ZrO_2 gate dielectric over the same time period.

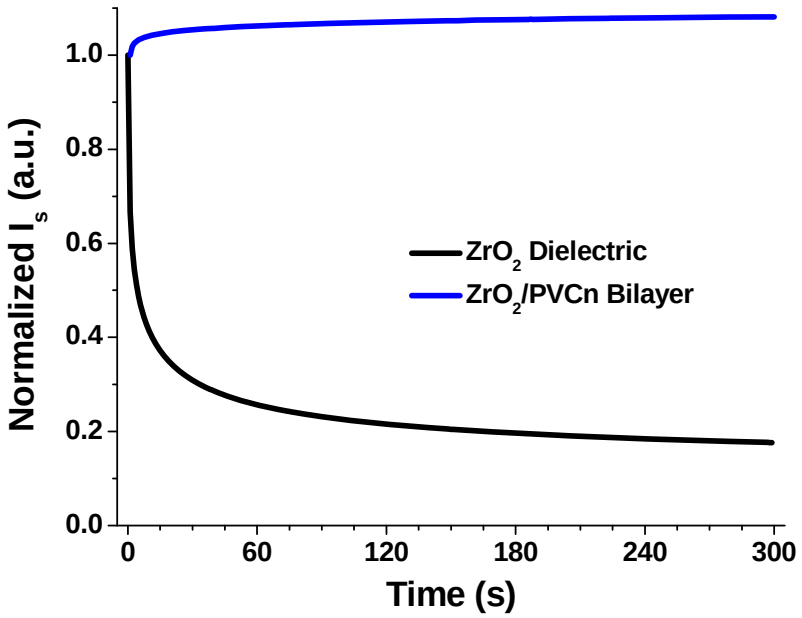

Figure 14: Bias stress effect in devices both with and without a thin PVCn bilayer dielectric. The device with the PVCn displayed an increase in drain current over time, with a total change of roughly 5% over 5 minutes. This compares to a reduction of 80% over the same timeframe using just ZrO_2 as the gate dielectric.

4 Alternative Bilayer Dielectrics

A similar approach was used previously on a semiconductor provided by Mitsubishi Co. using a porphyrin-based approach to produce a high-mobility p-type material. In this study, electron beam evaporation and plasma-enhanced chemical vapor

deposition (PECVD) were used to create a bilayer metal-oxide dielectric. A tantalum oxide (Ta_2O_5) insulator was first deposited on a heavily doped silicon wafer by e-beam evaporation. A thin second insulating layer of silicon dioxide was then deposited by PECVD.

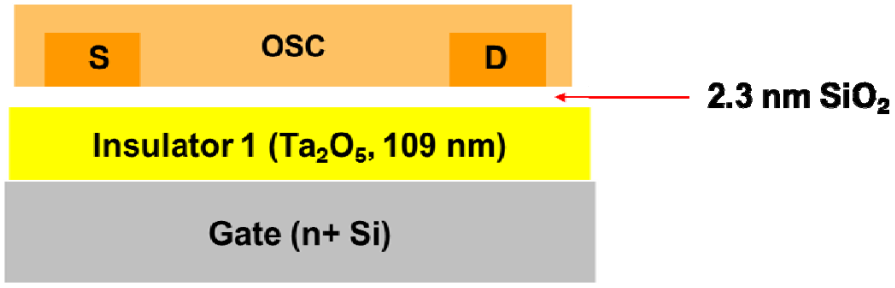

Figure 15: Bilayer dielectric device structure using e-beam deposited Ta_2O_5 and PECVD deposited SiO_2.

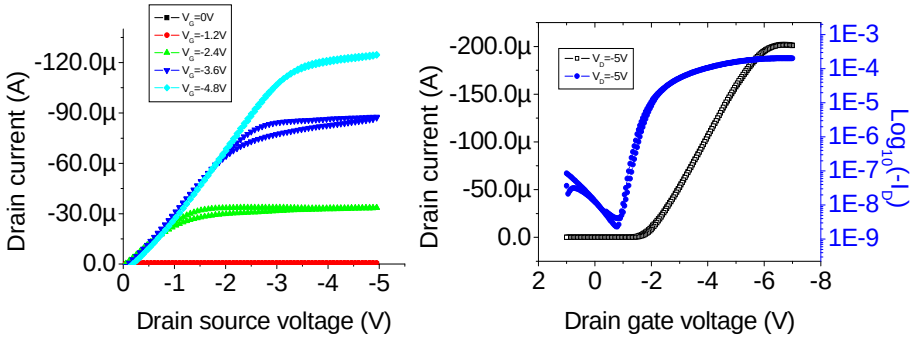

Figure 16: Output and transfer curves for devices with a bilayer Ta_2O_5/SiO_2 dielectric.

The resulting output and transfer curves can be seen in Figure 16. At longer channel lengths, these devices exhibited carrier mobilities of up to 1.36 cm2/Vs. Devices were also fabricated without the addition of the thin SiO_2 layer; however, field effect

mobilities of less than 0.5 cm^2/Vs were obtained. Similar mobility reductions in the presence of a highly polar gate insulator have been documented previously by Hulea *et al*. [8]. This difference is associated with a phenomenon known as a Fröhlich polaron, where a charge carrier induces a local shift in its polar surroundings, resulting in an increased reorganization energy being needed to move.

The absence of such a large shift in mobility in the previous pentacene-based devices is attributed to the relatively lower carrier mobilities within those devices. The barrier height resulting from grain boundaries and other forms of disorder is the limiting factor for transport through the material, overwhelming any Fröhlich polaron effects, which are seen primarily in high-mobility poly-crystalline and single-crystal organic semiconductors.

5 FIGURE OF MERIT

When comparing device performance, carrier mobility is the oft-quoted metric by which an organic semiconductor is judged. However, when judging the usefulness of a device for a particular application, what is of interest is the necessary voltage change required in order to realize a desired change in current. The single largest contributing factor to this value, aside from carrier mobility, is the capacitance of the gate dielectric. In addition, the carrier mobility may change based on the device structure employed, as shown above. It may also change based on the sheet carrier density (modulated by the applied gate voltage), a common feature in disordered semiconductors, as shown in Figure 7. Therefore, we propose a figure of merit that reflects the quality of the semiconductor-insulator combination as a whole.

Conductivity is directly related to sheet charge density ($\sigma = q*\mu*n$), and the charge density per unit area is determined by the applied gate voltage and the capacitance of the gate dielectric ($n = C_i*V_G$). We would like to compare material systems without looking at the particulars of device geometry, however, so the relative dielectric constant of the insulator is a better value indicative of its inherent ability to induce a large carrier concentration. Carrier mobility multiplied by the dielectric constant of the insulator gives a single value that allows simple comparison across multiple material systems.

When applied to the aforementioned material systems, we find a Figure of Merit (FoM) of 8 for the pentacene devices employing a ZrO_2/PVCn bilayer dielectric, and a FoM of 35 for the porphyrin-based semiconductor using the Ta_2O_5/SiO_2 bilayer. Devices fabricated using these semiconductors using pure SiO2 gate dielectrics, on the other hand, exhibited FoM values of 1.3 and 1.9, respectively.

6 SUMMARY

The fabrication of organic transistors that operate at relatively low voltages, in this case less than 5 V, is of large importance in order to make these devices useful in realistic applications. This work demonstrates the fabrication of low voltage pentacene devices using a high dielectric constant insulator (ZrO_2) and demonstrates solutions to problems that this choice of insulator introduces.

The addition of a thin layer of a hydrophobic polymer insulator on top of the ZrO_2 dramatically reduces bias stress effects in the device. Poly(vinyl cinnamate) proves to be an extremely useful choice for this insulator. It allows simple deposition from solution

and, once cross-linked, becomes insoluble to a large variety of common solvents. This allows the use of traditional photolithography techniques on top of this layer, or the deposition of semiconducting layers from solution without worrying about the solvent used for the semiconductor damaging the underlying layer.

A similar approach has also been demonstrated for devices using a high-mobility semiconductor and a bilayer dielectric consisting of Ta_2O_5 and a thin SiO_2 interfacial layer. The improved device performance in both cases utilizing the high-k gate insulator has led to our proposal of a unique Figure of Merit that describes the material combination of both semiconductor and insulator. Due in large part to the high carrier mobility achieved using this bilayer dielectric approach, we have shown a FoM that exceeds that achieved in published reports on single crystal devices.

References

1. Seon, J.-B., et al., *Spin-Coated CdS Thin Films for n-Channel Thin Film Transistors.* Chemistry of Materials, 2009. **21**(4): p. 604-611.
2. Lee, C., Dodabalapur, A., *Solution-processed zinc-tin oxide thin-film transistors with high performance and improved uniformity.* Device Research Conference, 2010. p. 123-124.
3. Leauw, D.d. in *Materials Research Symposium*. 2010. San Francisco, USA.
4. Podzorov, V. in *Materials Research Symposium*. 2010. San Francisco, USA.
5. Sekitani, T., et al., *Suppression of DC bias stress-induced degradation of organic field-effect transistors using postannealing effects.* Applied Physics Letters, 2005. **87**(7): p. 073505-3.
6. Lee, C.A., et al., *Hysteresis mechanism and reduction method in the bottom-contact pentacene thin-film transistors with cross-linked poly(vinyl alcohol) gate insulator.* Applied Physics Letters, 2006. **88**(25): p. 252102-3.
7. Wang, A., et al., *Tunable threshold voltage and flatband voltage in pentacene field effect transistors.* Applied Physics Letters, 2006. **89**(11): p. 112109-3.
8. Hulea, I.N., Fratini, S., Xie, H., et al. *Tunable Fröhlich polarons in organic single-crystal transistors.* Nature Materials, 2006. **5**(12): p. 982-986.